REMARKS

Claims 1-5 remain pending in the application. Claim 1 has been amended without introduction of new matter. Favorable reconsideration is respectfully requested in view of the above amendments and the following remarks.

The specification has been amended at page 3, line 34, to correct a typographical error. In particular, the word "pf" has been changed so that it now reads "of" select. No new matter has been introduced by this amendment.

The drawings were objected to as being informal, but were deemed acceptable for examination purposes only. The Office stated that formal drawings will be required when the application is allowed. Accordingly, no new drawings are presented at this time.

Claims 1-5 stand rejected under 35 USC §102(e) as allegedly being anticipated by Mattisson et al. (US Patent 6,690,740 B1). This rejection is respectfully traversed.

The invention relates to techniques and apparatuses for estimating DC offsets in a received signal in a communication system. As explained in the Background section, there will be frequency offsets in an FM-modulated received signal which are due to various imperfections at both the transmitter and the receiver. This means that the output from an FM detector will not be zero for an un-modulated carrier, and therefore zero cannot be used as a threshold to make a decision at the output of the FM detector. By estimating the DC offset in the received signal, a proper choice of threshold may be determined.

The application describes two different DC estimation methods. First, a coarse DC offset estimation is found using the packet preamble. In an aspect of the invention, the preamble need not be DC free. The course estimation involves a diode circuit.

Second, the diode circuit is switched out and a second mechanism is used (e.g., a low pass filter) to provide a DC offset estimate of the essentially DC-free data part of the packet.

As now amended, independent claim 1 not only defines that the estimation method used during reception of a preamble part of the input signal "does not rely on a DC-free signal to estimate the DC offset value of the input signal", but now also expressly states that "a different estimation method" is used during reception of the data part of the input signal, the different estimation method being one "which relies on a DC-free signal to estimate the DC offset value of the input signal." These two points are novel and nonobvious over the Mattisson et al. document at least because Mattisson et al. uses an estimation method which, during reception of a preamble part of the input signal does rely on a DC-free signal to

estimate the DC offset value, and because Mattisson et al. use a same estimation method for estimating the DC offset value of the input signal during both reception of a preamble part and reception of the data part of the input signal.

More particularly, Mattisson et al. describe a multi-part digital preamble for use in transmitting digital data packets. An exemplary three-part preamble in accordance with Mattisson et al. is depicted in FIG. 5 and described at column 6, lines 25-39. According to Mattisson et al., the three-part preamble 500 includes a DC-free leading sequence 510, followed by a multiple-bit synchronization word 520 which is not necessarily DC-free and which can be different for each data packet. The synchronization word 520 is in turn followed by a trailing DC-free sequence 530. As stated by Mattisson et al. at column 6, lines 40 *et seq.* the leading DC-free sequence 510 induces a coarse estimate of the baseband DC offset on the storage capacitor 340. This course estimate is then used to permit successful detection of the coded synchronization word 520. The trailing DC-free sequence 530 is subsequently used as the basis for determining an accurate estimate of the DC offset for reception and detection of the incoming digital data packet.

Thus, two DC-free parts of the preamble provide the DC offset estimate. The remainder of the preamble 500 is the synchronization word 520 which is not necessarily DC-free. However, the synchronization word 520 is not used to estimate the DC-offset. Hence, the parts of the packet used to provide a DC offset estimate are DC-free, in contrast to the method defined by claim 1 of the present application.

Considering other aspects of the Mattisson et al. patent, FIG. 3 is included in order to demonstrate the problems associated with the prior art, as explained in columns 5 and 6. It assumes that the DC offset is estimated using a DC-free preamble, and after the preamble is found, the DC offset estimate is stored for reception and detection of the incoming data packet through the opening of switch 330. Hence, in contrast to the method defined by claim 1, there are not two different estimation methods used for the preamble and data parts of the packet.

FIG. 6 of Mattisson et al. again includes a storage switch 330 that can be opened once a DC offset estimate has been established. The DC offset is then updated. The switch prior to the estimation circuit is present so that the DC offset estimate is updated only when the received signal is of sufficient strength. Hence, neither switch present in FIG. 6 performs the function of the switch present in FIG. 1 of the present application, that is, to switch out part

of the circuit in order for a different estimation method to take place for the data part of the packet.

Claim 1 is therefore believed to be novel and nonobvious over the Mattisson et al. document for at least the foregoing reasons.

Turning now to claims 2-5, these claims specifically define various circuits and components used for carrying out steps of the estimation. A diode arrangement provides a coarse estimate of the DC offset value of the preamble signal. The diode arrangement is then switched out, and the remaining low pass filter provides an estimate of the DC offset value of the data part of the signal.

Independent claim 2 defines an arrangement whereby estimating a DC offset value of the preamble portion of the input signal is performed "using a resistance and first and second diodes connected in parallel, the input signal being supplied to one terminal of the resistance, to the anode of the first diode and to the cathode of the second diode, and the DC estimate being supplied from a terminal connected with another terminal of the resistance, with the cathode of the first diode and with the anode of the second diode." Estimating a DC offset value of the data part of the input signal is performed "using a low pass filter which includes the said resistance." (Emphasis added.)

Independent claim 4 defines "a circuit for estimating a DC offset value of an input signal comprising: input and output terminals; a low pass filter including a resistor and a capacitor, the resistor being connected between the input and output terminals and the capacitor being connected between the output terminal and ground; a pair of diodes operatively connected in parallel between the input and output terminals of the circuit, the first diode having its anode connected to the input terminal and its cathode connected to the output terminal, and the second diode having its cathode connected to the input terminal and its anode connected to the output terminal; and switch means operable to switch a connection to the output terminal, such that the pair of diodes is connected to the output terminal during receipt of a preamble part of an input signal, and is not connected to the output terminal during receipt of a data part of the input signal subsequent to the preamble part thereof." (Emphasis added.)

Independent claim 5 defines "a circuit for estimating a DC offset level of an input signal, the circuit comprising: input and output terminals; a capacitance connected between the output terminal and ground; a control unit having an input, and an output which is

connected with the output terminal; a resistance connected between the input terminal and the output terminal; a first diode having its anode connected with the input terminal and its cathode connected with the input of the control unit; and a second diode having its cathode connected with the input terminal and its anode connected with the input of the control unit; wherein the control unit is operable to selectively connect its input to the output terminal, such that the first and second diodes are connected to the output terminal during receipt of a preamble part of an input signal, and such that the first and second diodes are not connected to the output terminal during receipt of a data part of the input signal subsequent to the preamble part thereof." (Emphasis added.)

The Mattisson et al. patent does not disclose a comparable resistor, capacitor, diode-pair arrangement. The Office relies on FIG. 6 of Mattisson et al. in support of its rejections, but this reliance is unfounded because the arrangement depicted in FIG. 6 does not satisfy all of the limitations of Applicants' claims. For example, each of claims 2, 4, and 5 requires that the anode of the first diode and the cathode of the second diode both be connected to the same input terminal, and that the cathode of the first diode and the anode of the second diode both be connected to a same connection point (an output terminal in claims 2 and 4, and a control unit input in claim 5). By contrast, Mattisson et al.'s FIG. 6 discloses an arrangement wherein an anode of the diode 610 and a cathode of the diode 620 are both connected to a common input terminal, but wherein the cathode of the diode 610 is connected to a terminal of a capacitor 670 and the anode of the diode 620 is connected to a different terminal of a different capacitor 680. Other differences between the arrangement depicted in Mattisson et al.'s FIG. 6 and Applicants' various claimed embodiments may be found. For example, Mattisson et al. do not show "a resistance and first and second diodes connected in parallel" (claim 2) or a "resistor being connected between the input and output terminals" (claims 4 and 5).

The various differences between Applicants' claimed embodiments and the arrangement shown in the Mattisson et al. patent are not insignificant because they are intended to operate in very different ways. In Mattisson et al., a method is provided of estimating the DC-offset by averaging the maximum and minimum values of the detected signals. A positive peak detector circuit and a negative peak detector circuit provide positive and negative envelopes, which are then averaged when switch 330 is closed, providing an

estimate of the DC offset. Hence, the diode arrangement in FIG. 1 of the present application is for a very different purpose from the diode arrangement in FIG. 6 of Mattisson et al.

Furthermore, in FIG. 6 of Mattisson et al., it is apparent that there is essentially no change of time constant. The estimation is carried out, and once the correlation is found, the obtained DC estimate is used throughout the packet. By contrast, in the invention as defined by Applicants' claims, the time constant is switched to a larger one, constantly updating the DC estimate during the reception of the packet. The use of a larger time constant also allows a possible frequency drift (the changing of the frequency offset throughout the packet) to be tracked.

The various arrangements defined by claims 2-5 also enable a DC offset value to be obtained from the first and second diode combination during receipt of the preamble part of the input signal, and from the low pass filter during receipt of the data part of the input signal. This feature is not disclosed in Mattisson et al.

For at least the foregoing reasons, claims 2-5 are believed to be novel and nonobvious over Mattisson et al.

In view of the above, it is respectfully asserted that claims 1-5 are patentable. It is therefore respectfully requested that the rejection of these claims under 35 USC §102(e) be withdrawn.

The application is believed to be in condition for allowance. Prompt notice of same is respectfully requested.

Respectfully submitted,
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